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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/814,021	03/31/2004	Ralf Killig	20 020709	5516

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EXAMINER	
NGUYEN, LINH M	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/814,021	KILLIG, RALF	
	Examiner	Art Unit	
	Linh M. Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004 and 09 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,17,18 and 20-26* is/are rejected.

7)☒ Claim(s) *10-16 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03/31/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-26 are presented in the instant application according to the Applicants' filing on 03/31/2004.

Claim Objections/Minor Informalities

1. Claims 3-5, 7, 9, 12, 16, 19, and 21-23 are objected to because of the following informalities:

Change "adapted" to -- configured-- to reflect positive limitations, as follow:

Claim 3, line 2;

Claim 4, line 1;

Claim 5, line 1;

Claim 7, line 2;

Claim 9, line 2;

Claim 12, line 2;

Claim 16, line 2;

Claim 21, line 2;

Claim 22, line 4;

Claim 23, lines 1, 3 and 5;

Claim 19, it is suggested to change "7" (in line 1) to --12-- to resolve antecedent basis issue regarding "said second superior counters" in line 2.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9, 17-18 and 23-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Parks (U.S. Patent No. 5,535,377).

With respect to claims 1, 23, and 24, Parks discloses, in Figs. 1-3, col. 5, lines 12-16, an apparatus for supplying a plurality of clock signals, the apparatus comprising a set of clock signal circuits [Fig. 2] for generating m clock signals of at least two different signal periods [Fast, Slow], with m being a natural number, a superperiod signal generating unit [PLL] for deriving, from a dedicated clock signal of said set of clock signals, a first superperiod signal [base], whereby the signal period of the first superperiod signal is a common multiple of the clock signals' signal periods [col. 5, lines 12-16].

With respect to claim 2, Parks discloses, in Figs. 1-3, col. 5, lines 12-16, that one signal period of the first superperiod signal comprises n_i signal periods of the respective i-th clock signal, whereby n_i is a natural number, and $1 \leq i \leq m$.

With respect to claims 3 and 25, Parks discloses, in Fig. 2, that at least some of the clock signal circuits comprise synchronization facilities [Fig. 2] for synchronizing at least some of the clock signals to the first superperiod signal.

With respect to claim 4, Parks discloses, in Fig. 1, a central facility [122] for programming or reprogramming the respective value n_i corresponding to the i-th clock signal, for any i with $1 \leq i \leq m$.

With respect to claim 5, Parks discloses, in Fig. 1, a central facility [122] for programming or reprogramming at least one of the clock frequency of the i-th clock signal, for any i with $1 \leq i \leq m$ or the respective value n_i corresponding to the i-th clock signal.

With respect to claim 6, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, that the signal period of the first superperiod signal [base] is the lowest common multiple of the clock signals' [fast, slow] signal periods.

With respect to claim 7, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, that the superperiod generating unit comprises a first superperiod counter [620] for generating one superperiod of the first superperiod signal per nj signal periods of the dedicated j-th clock signal.

With respect to claim 8, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, that at least some of the clock signal circuits delay their respective clock signal in a way that at least some of the edges of the respective clock signal coincide with edges of the first superperiod signal.

With respect to claim 9, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, that at least some of the clock signal circuits comprise variable delay elements for compensating the relative phase delay between the respective clock signal and the first superperiod signal.

With respect to claim 17, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, that at least some of the clock signal circuits comprise clock selection facilities [402] that allow to select,

besides the clock signal circuit's own clock signal, a clock signal of a remote clock signal circuit as an output signal of the clock signal circuit.

With respect to claim 18, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, that any clock signal of the set of clock signals is selectable as the dedicated clock signal.

With respect to claim 26, Parks discloses, in Figs. 1-3 and col. 5, lines 12-16, an apparatus with a software program or product, preferably stored on a data carrier, for executing the steps of generating m clock signals [fast, slow] of at least two different signal periods, with m being a natural number; deriving, from a dedicated clock signal of the set of clock signals, a first superperiod signal [base], whereby the signal period of said first superperiod signal is a common multiple of the clock signals' signal periods [col. 5, lines 12-16] when run on a data processing system such as a computer.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Parks (U.S. Patent No. 5,535,377) in view of Bristow et al. (U.S. Patent No. 6,754,868).

With respect to claim 20-21, Parks discloses all of the claimed limitations as expressly recited in claim 1.

Parks fails to explicitly disclose that the clock signals are utilized in a DUT testing environment for at least one of providing stimulus signals to a DUT and receiving response signals from the DUT.

Bristow et al. discloses, in Figs. 9 and 10, and col. 3, line 19-32, in a DUT testing environment for at least one of providing stimulus signals to a DUT and receiving response signals from the DUT.

To configure the circuit of Parks with an automated test equipment for testing at least one DUT as taught by Bristow et al. to at least provide the ability to couple any output on a pattern generator to any pin on a DUT, and to switch the signal coupled to the pin at least twice in each clock cycle would have been obvious to one of ordinary skill in the art at the time of the invention since Bristow et al. teaches that by doing so would facilitate the ability to quickly and easily link multiple test sites *(see Bristow et al., col. 4, lines 1-17).*

With respect to claim 22, the combined teaching of Parks and Bristow et al. discloses that at least one of the clock frequency of the i-th clock signal, for any i with $1 < i$ S m, or the respective value n_i corresponding to the i-th clock signal, for any i with $1 \leq i \leq m$.

Allowable Subject Matter

6. Claims 10-16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 19 would be objected if corrected to overcome the objection set forth in this office action.

7. The following is a statement of reasons for the indication of allowable subject matter:

The closest prior art of record does not show or fairly suggest an apparatus, in which at least some of the clock signal circuits derive second superperiod signals from the respective clock signals and synchronize the second superperiod signals to said first superperiod signal, as called for in claim 10;

Inquiry

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linh M. Nguyen whose telephone number is (571) 272-1749. The examiner can normally be reached on Alternate Mon, Tuesday - Friday from 7:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LMN

LINH MY NGUYEN
PRIMARY EXAMINER